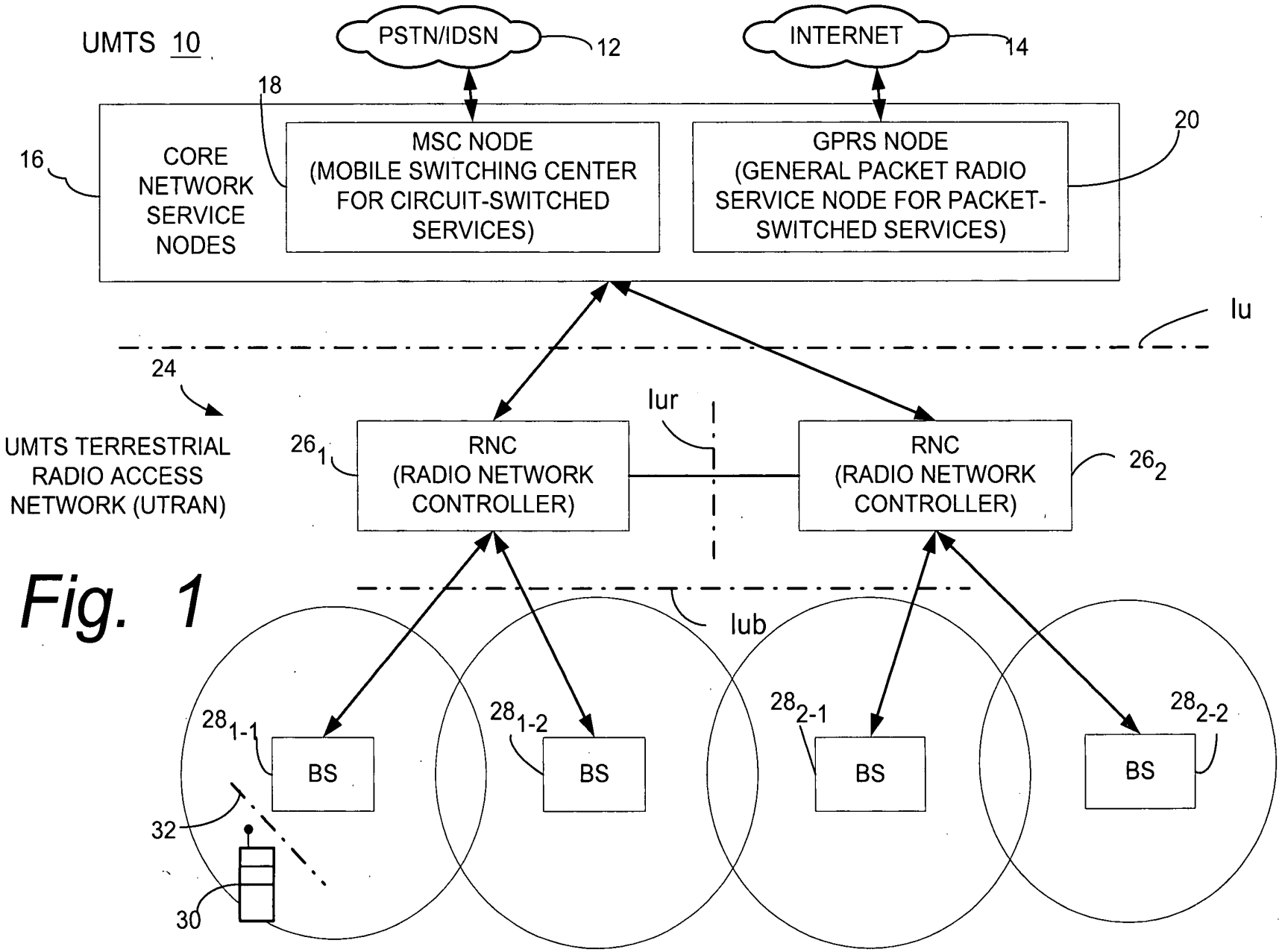

Fig. 1

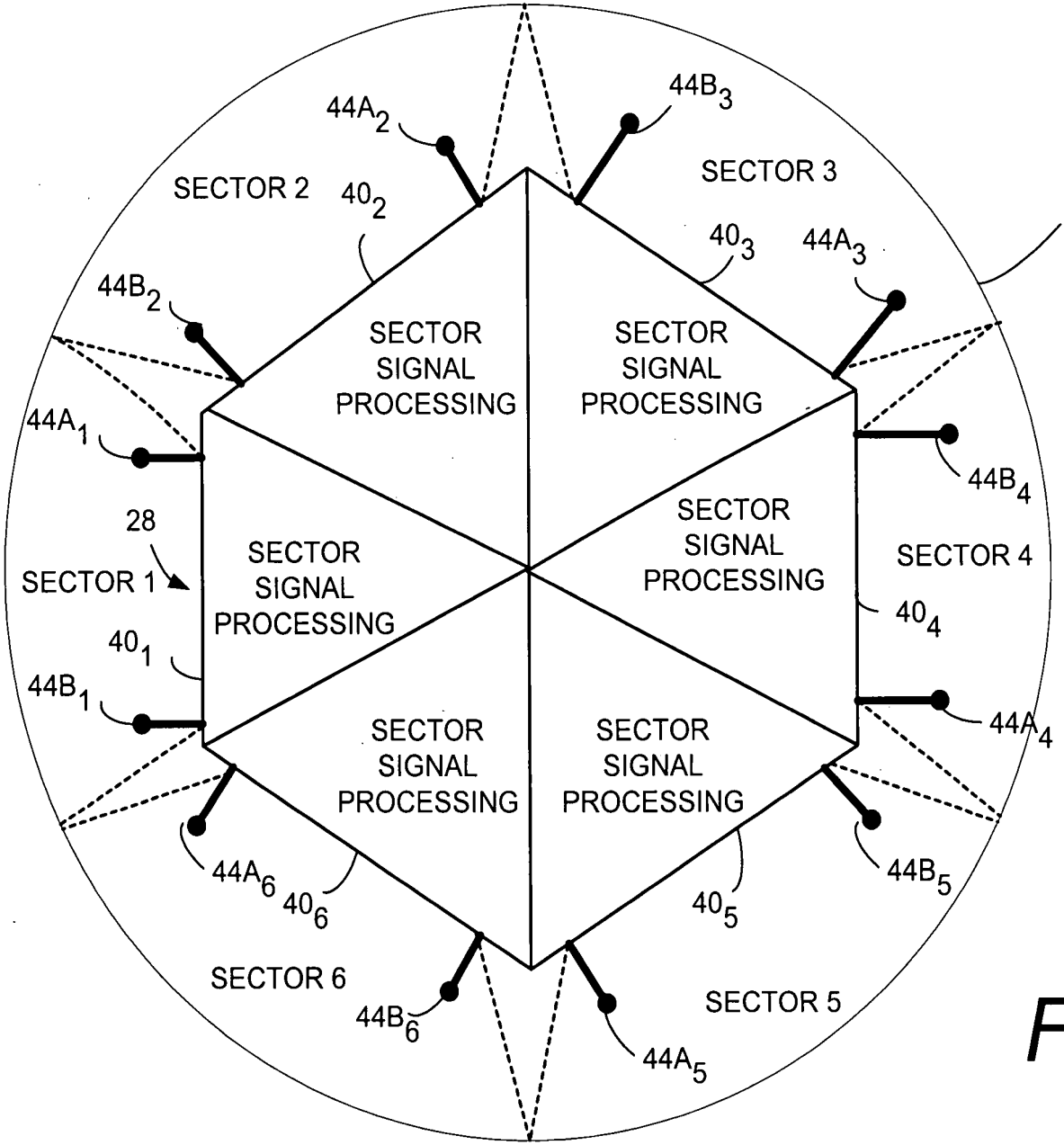

Fig. 2

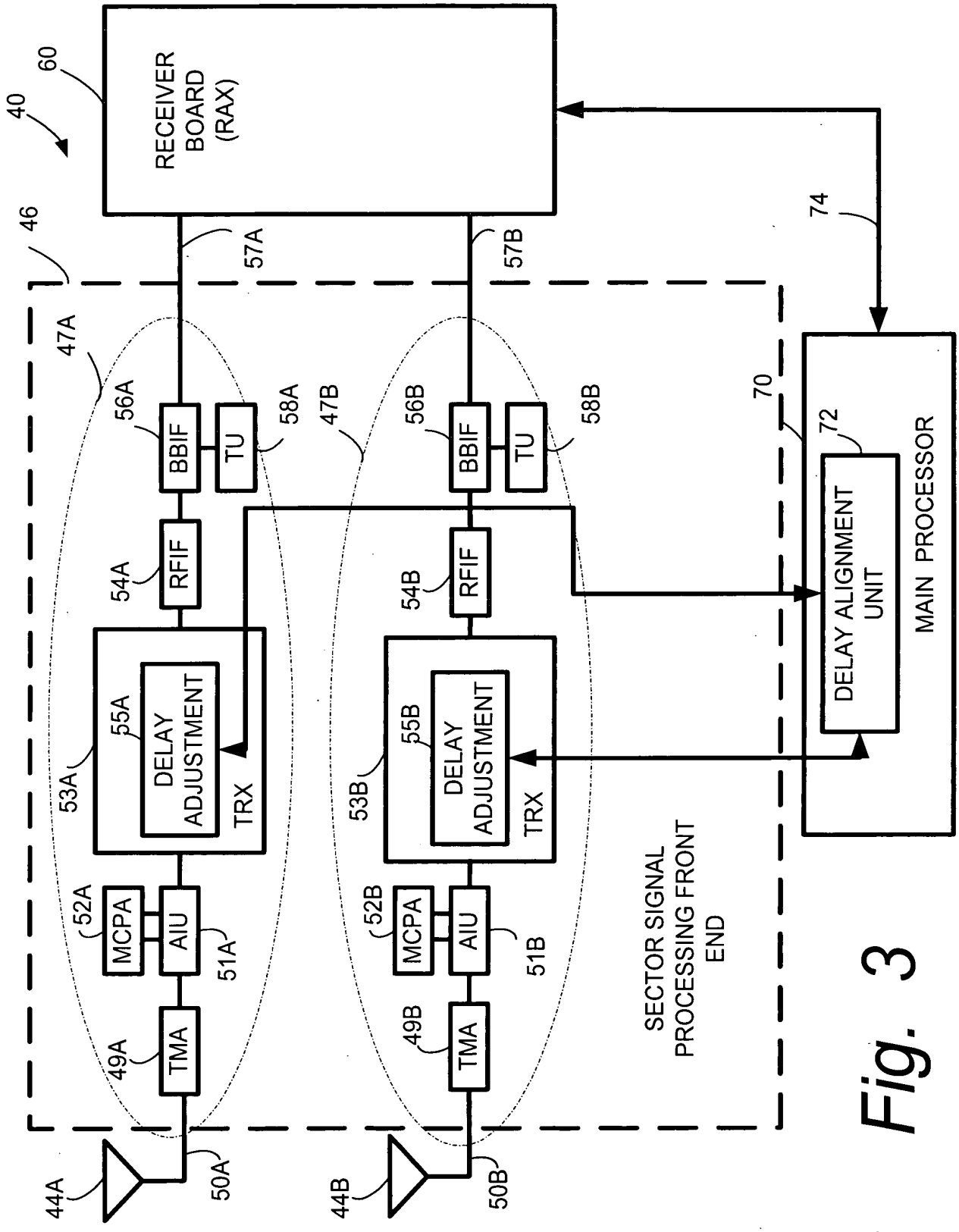
40
60
RECEIVER BOARD (RAX)
46
57A
57B
74
47A
47B
56A
56B
BBIF
TU
58A
58B
54A
54B
RFIF
70
72
DELAY ALIGNMENT UNIT
MAIN PROCESSOR
53A
53B
55A
55B
DELAY ADJUSTMENT
TRX
52A
52B
MCPA
AIU
51A
51B
49A
49B
TMA
SECTOR SIGNAL PROCESSING FRONT END
44A
44B
50A
50B

Fig. 3

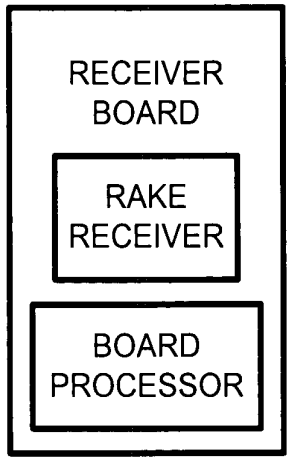

Fig. 4

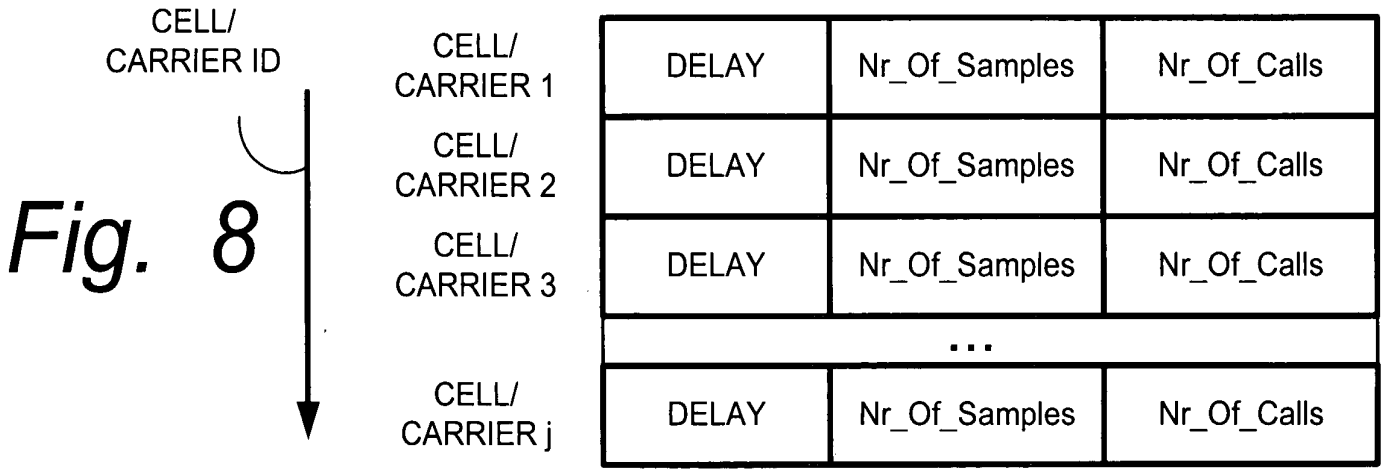

Fig. 8

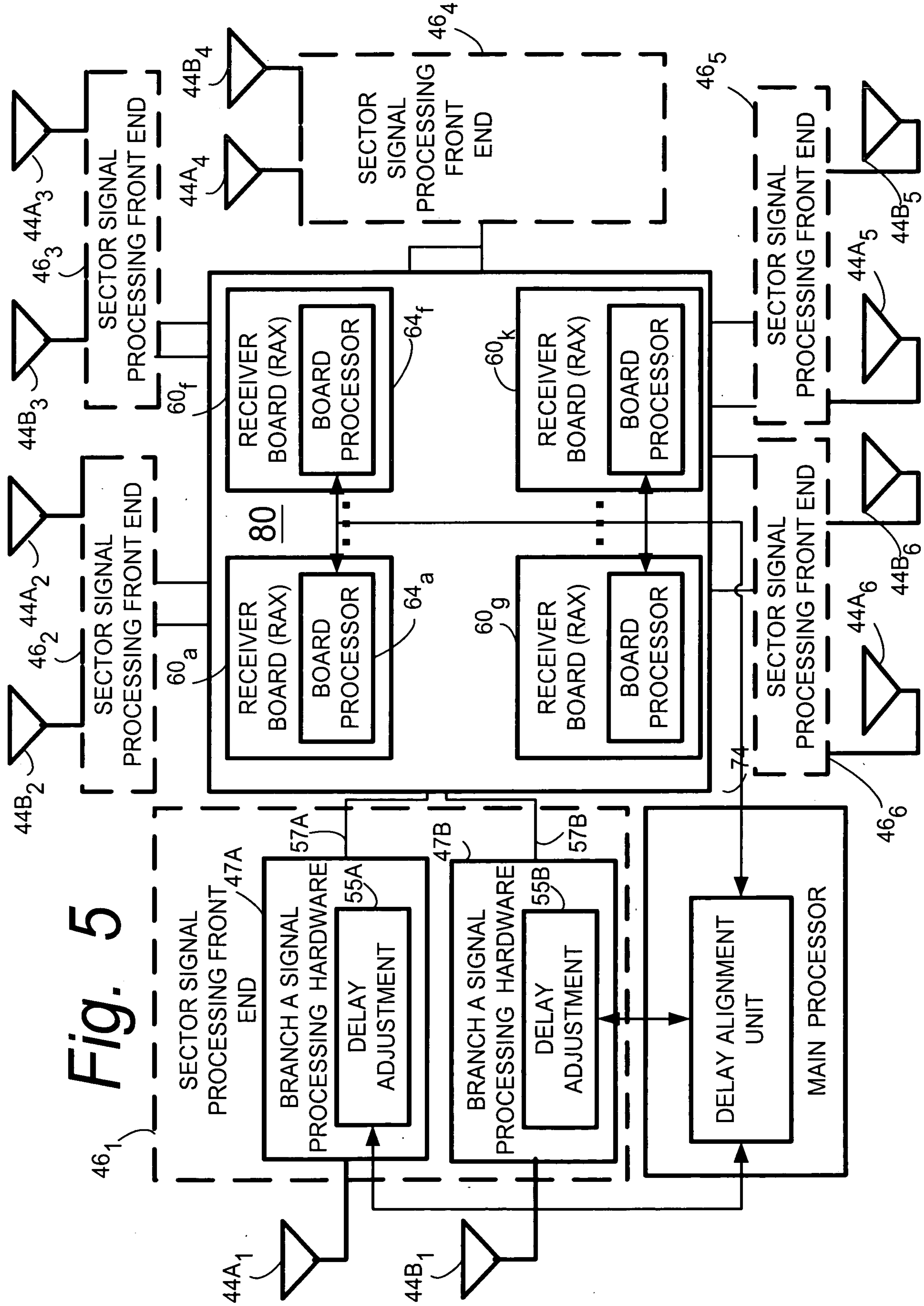
SECTOR SIGNAL PROCESSING FRONT END
RECEIVER BOARD (RAX)
BOARD PROCESSOR
80
BRANCH A SIGNAL PROCESSING HARDWARE
DELAY ADJUSTMENT
DELAY ALIGNMENT UNIT
MAIN PROCESSOR
44A1
44B1
44A2
44B2
44A3
44B3
44A4
44B4
44A5
44B5
44A6
44B6
461
462
463
464
465
466
47A
47B
55A
55B
57A
57B
60a
60f
60g
60k
64a
64f
74

Fig. 5

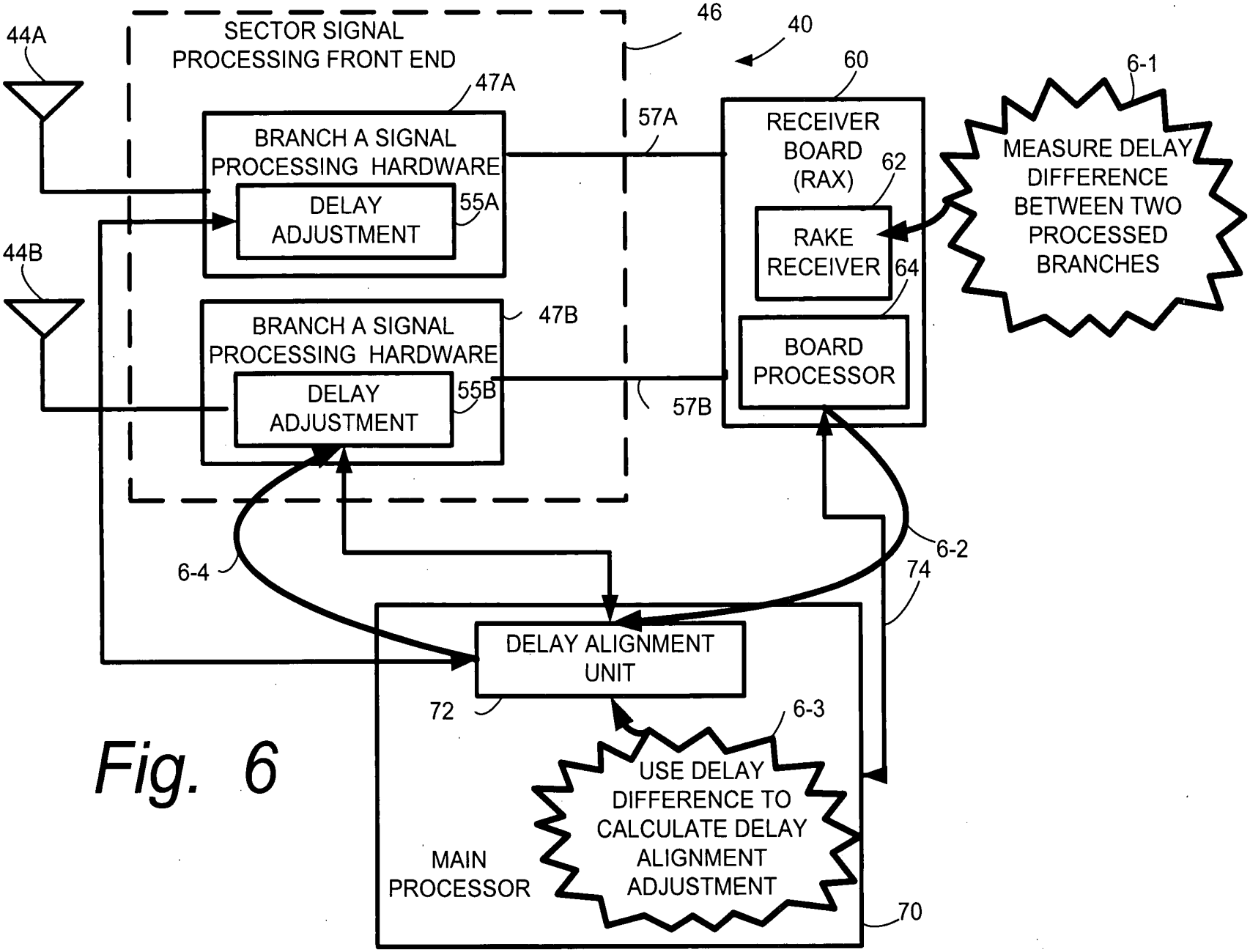

Fig. 6

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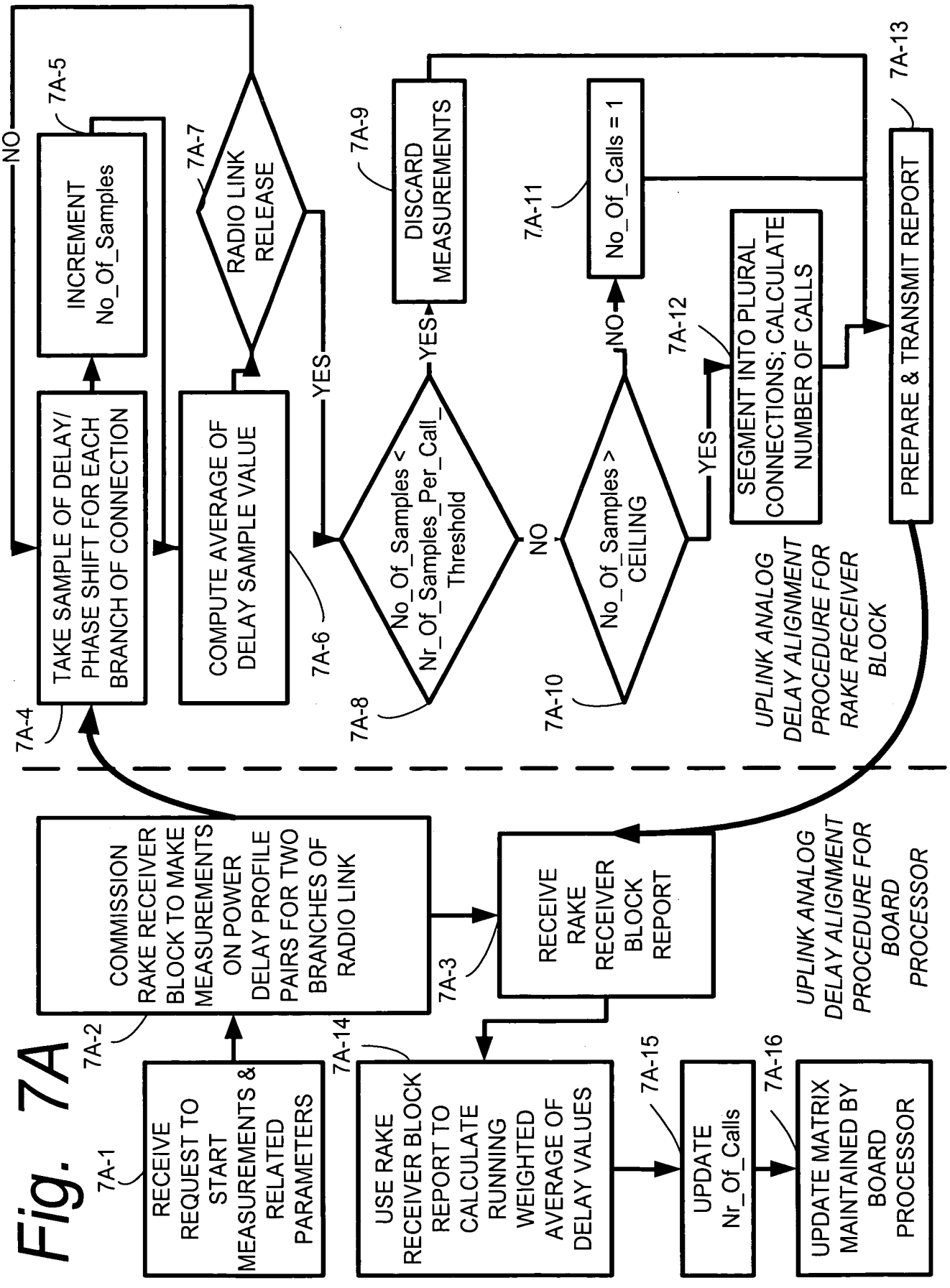
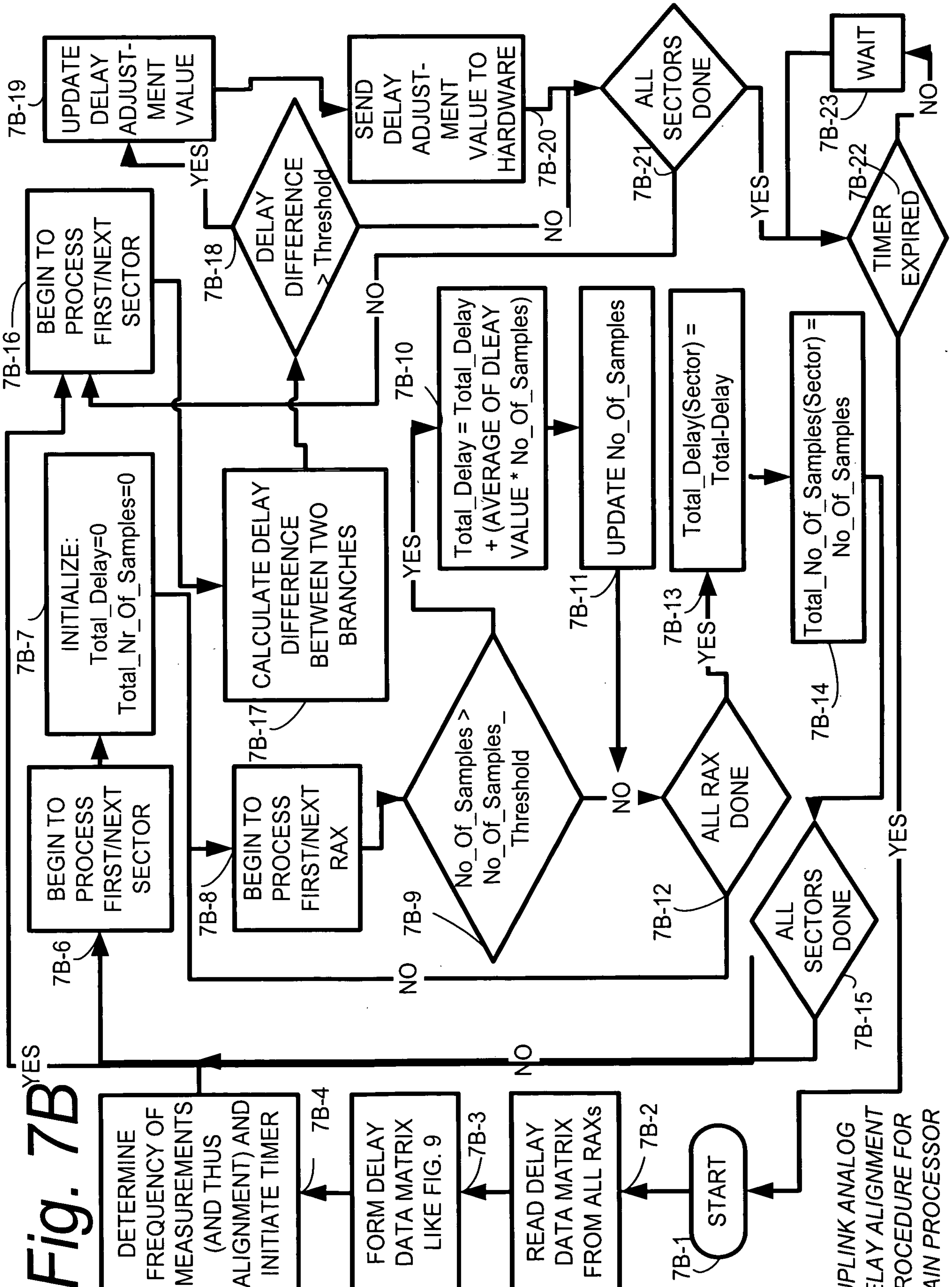


Fig. 7A

Fig. 7B


START
7B-1
READ DELAY DATA MATRIX FROM ALL RAXs
7B-2
FORM DELAY DATA MATRIX LIKE FIG. 9
7B-3
DETERMINE FREQUENCY OF MEASUREMENTS (AND THUS ALIGNMENT) AND INITIATE TIMER
7B-4
BEGIN TO PROCESS FIRST/NEXT SECTOR
7B-6
INITIALIZE: Total_Delay=0 Total_Nr_Of_Samples=0
7B-7
BEGIN TO PROCESS FIRST/NEXT RAX
7B-8
No_Of_Samples > No_Of_Samples_ Threshold
7B-9
Total_Delay = Total_Delay + (AVERAGE OF DLEAY VALUE * No_Of_Samples)
7B-10
UPDATE No_Of_Samples
7B-11
ALL RAX DONE
7B-12
Total_Delay(Sector) = Total-Delay
7B-13
Total_No_Of_Samples(Sector) = No_Of_Samples
7B-14
ALL SECTORS DONE
7B-15
BEGIN TO PROCESS FIRST/NEXT SECTOR
7B-16
CALCULATE DELAY DIFFERENCE BETWEEN TWO BRANCHES
7B-17
DELAY DIFFERENCE > Threshold
7B-18
UPDATE DELAY ADJUST-MENT VALUE
7B-19
SEND DELAY ADJUST-MENT VALUE TO HARDWARE
7B-20
ALL SECTORS DONE
7B-21
TIMER EXPIRED
7B-22
WAIT
7B-23
YES
NO

UPLINK ANALOG DELAY ALIGNMENT PROCEDURE FOR MAIN PROCESSOR

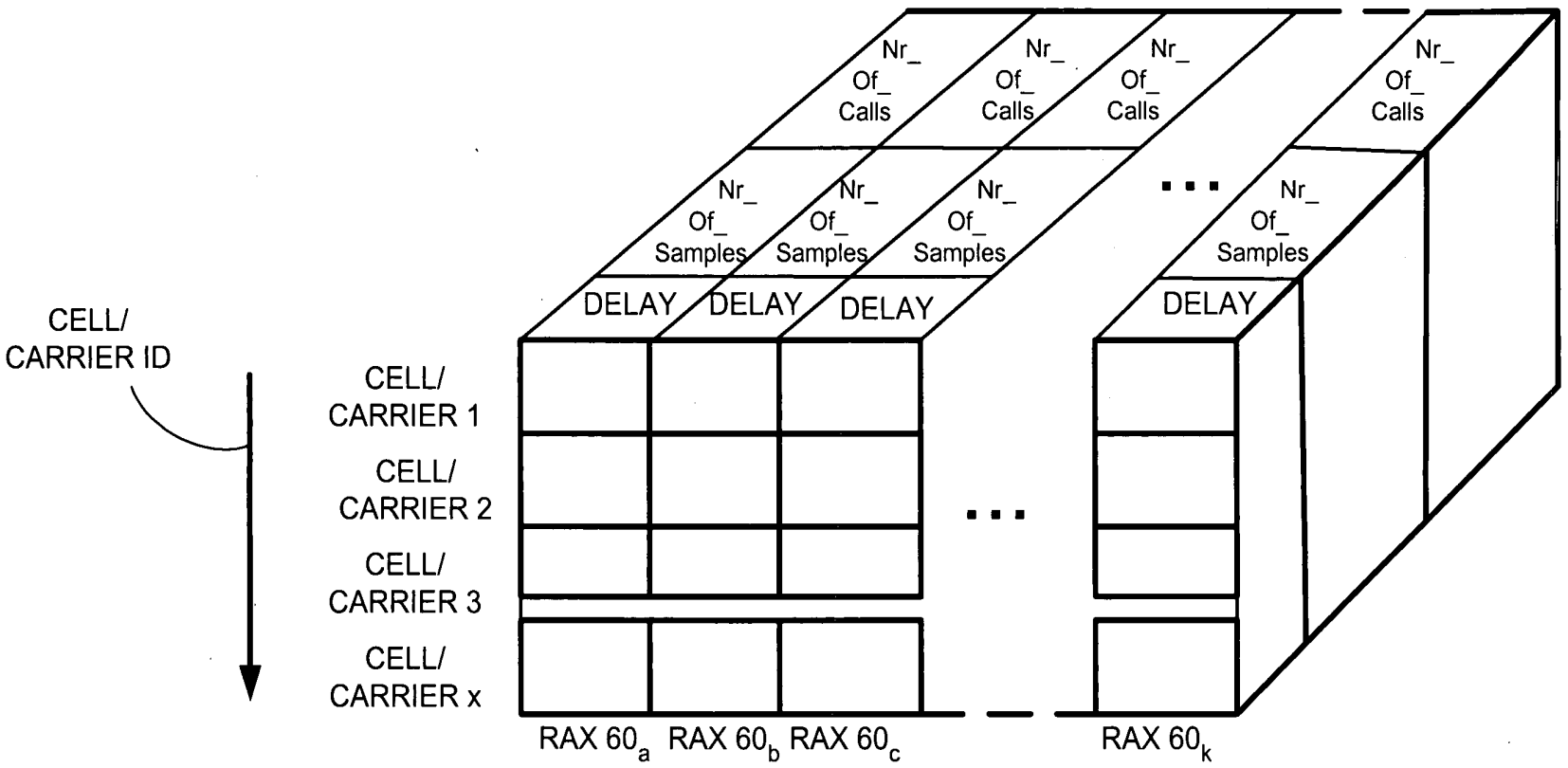


Fig. 9

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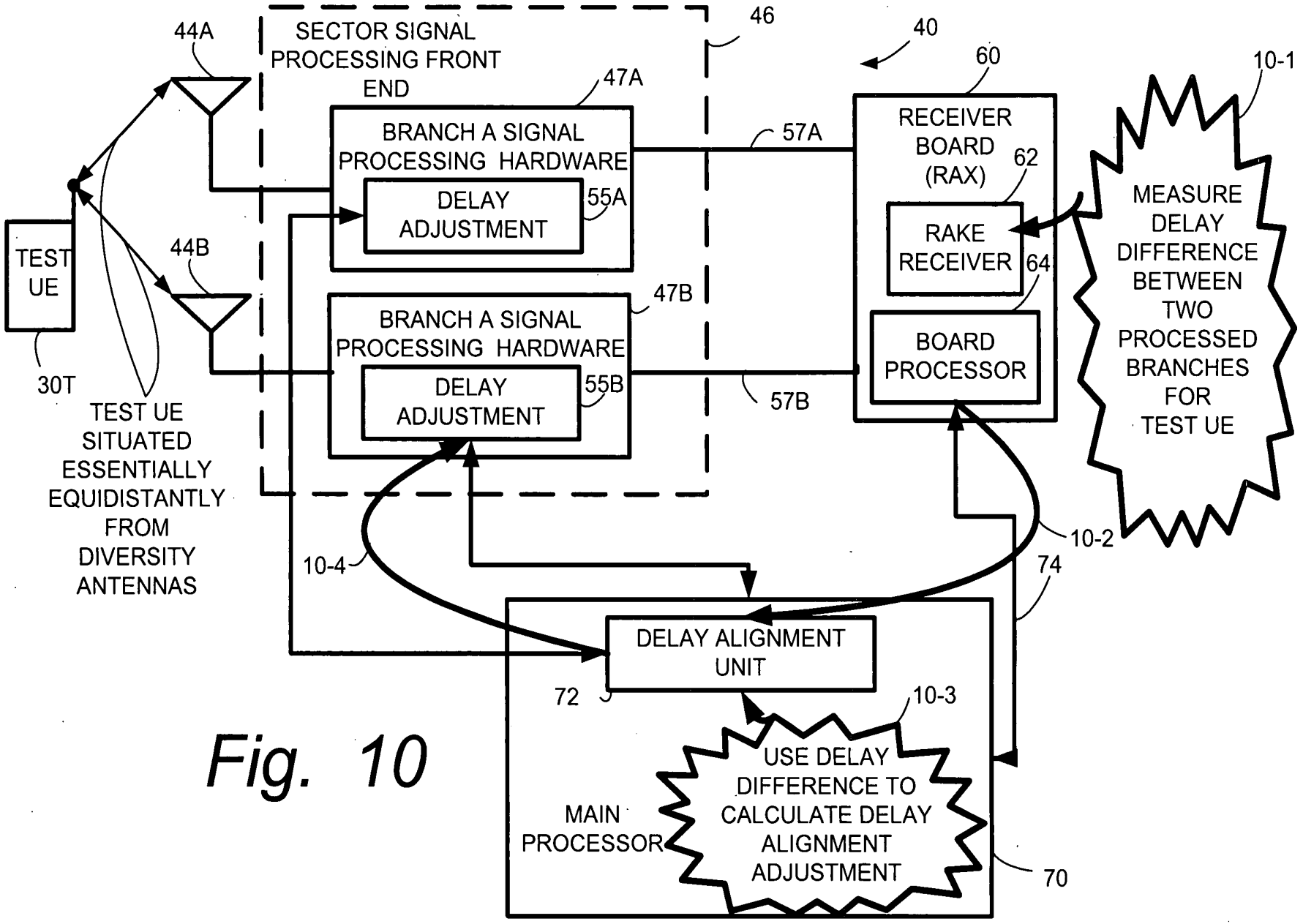

Fig. 10

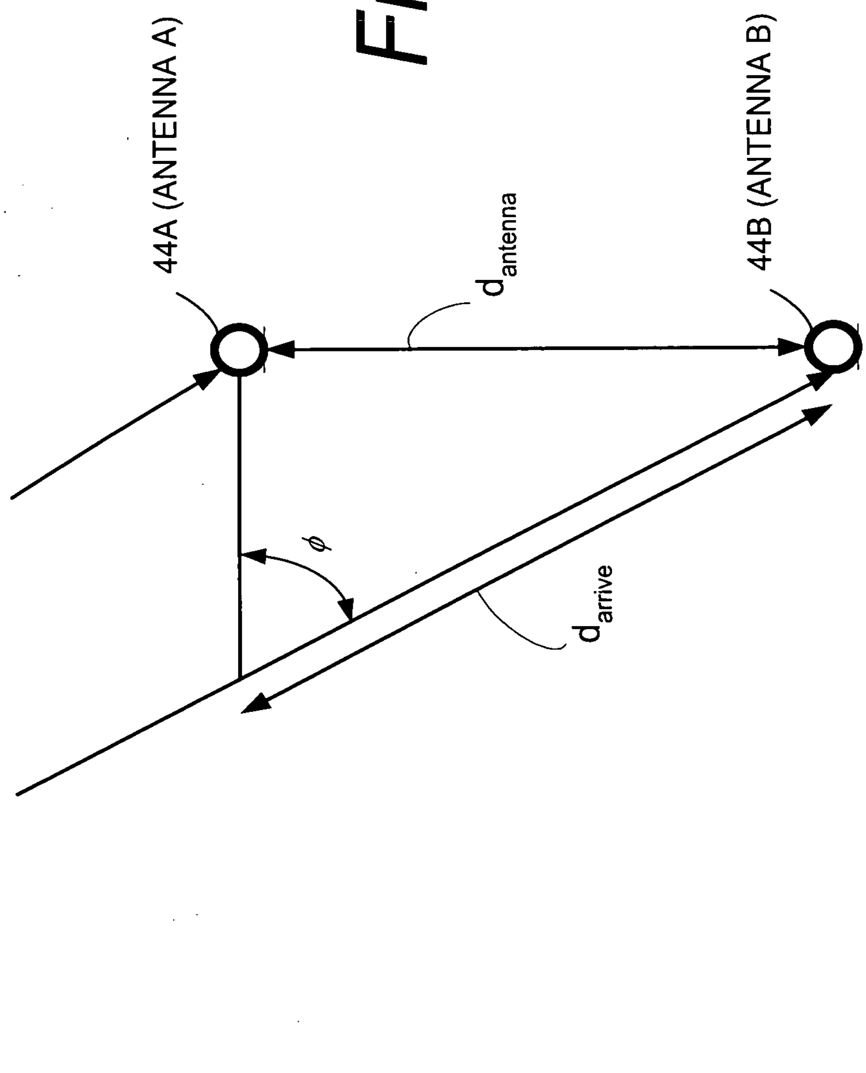

Fig. 11

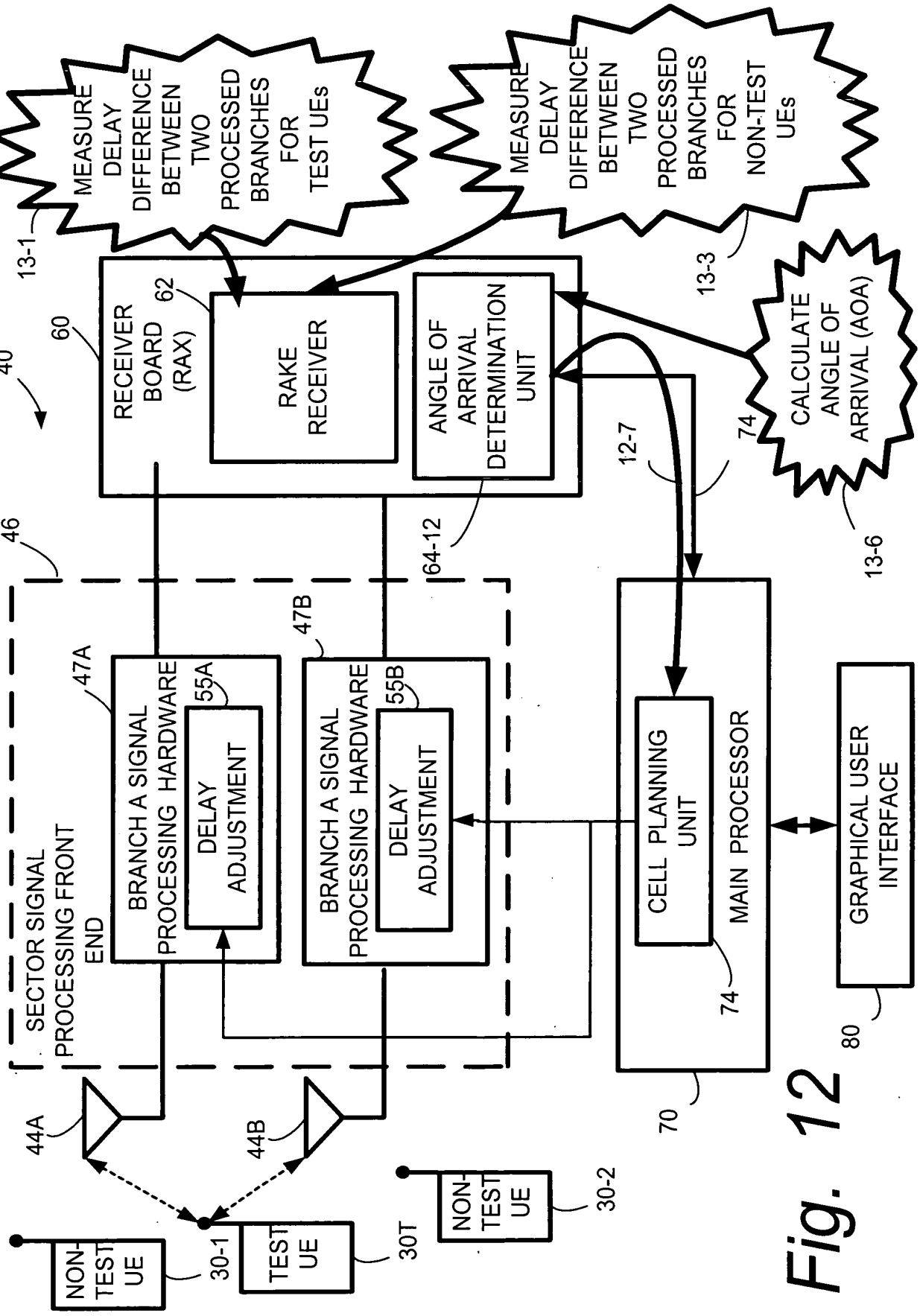
MEASURE DELAY DIFFERENCE BETWEEN TWO PROCESSED BRANCHES FOR TEST UEs
13-1
MEASURE DELAY DIFFERENCE BETWEEN TWO PROCESSED BRANCHES FOR NON-TEST UEs
13-3
CALCULATE ANGLE OF ARRIVAL (AOA)
13-6
74
40
RECEIVER BOARD (RAX)
60
62
RAKE RECEIVER
ANGLE OF ARRIVAL DETERMINATION UNIT
64-12
12-7
46
SECTOR SIGNAL PROCESSING FRONT END
47A
BRANCH A SIGNAL PROCESSING HARDWARE
55A
DELAY ADJUSTMENT
47B
BRANCH A SIGNAL PROCESSING HARDWARE
55B
DELAY ADJUSTMENT
CELL PLANNING UNIT
MAIN PROCESSOR
74
70
GRAPHICAL USER INTERFACE
80
44A
44B
NON-TEST UE
30-1
TEST UE
30T
NON-TEST UE
30-2

Fig. 12

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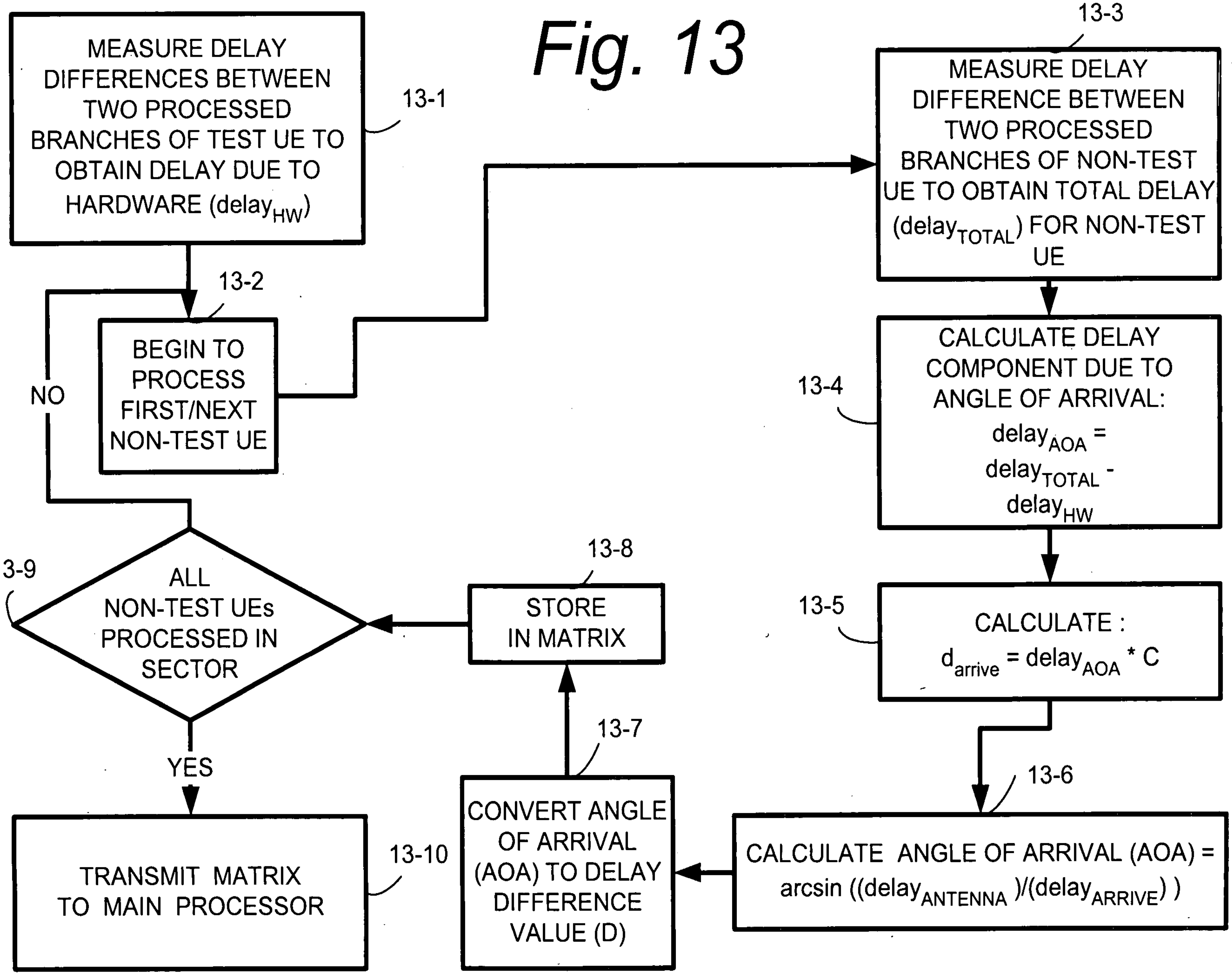
Fig. 13


MEASURE DELAY DIFFERENCES BETWEEN TWO PROCESSED BRANCHES OF TEST UE TO OBTAIN DELAY DUE TO HARDWARE (delay$_{HW}$)
13-1
13-2
BEGIN TO PROCESS FIRST/NEXT NON-TEST UE
13-3
MEASURE DELAY DIFFERENCE BETWEEN TWO PROCESSED BRANCHES OF NON-TEST UE TO OBTAIN TOTAL DELAY (delay$_{TOTAL}$) FOR NON-TEST UE
13-4
CALCULATE DELAY COMPONENT DUE TO ANGLE OF ARRIVAL: delay$_{AOA}$ = delay$_{TOTAL}$ - delay$_{HW}$
13-5
CALCULATE : d$_{arrive}$ = delay$_{AOA}$ * C
13-6
CALCULATE ANGLE OF ARRIVAL (AOA) = arcsin ((delay$_{ANTENNA}$)/(delay$_{ARRIVE}$))
13-7
CONVERT ANGLE OF ARRIVAL (AOA) TO DELAY DIFFERENCE VALUE (D)
13-8
STORE IN MATRIX
13-9
ALL NON-TEST UEs PROCESSED IN SECTOR
NO
YES
13-10
TRANSMIT MATRIX TO MAIN PROCESSOR

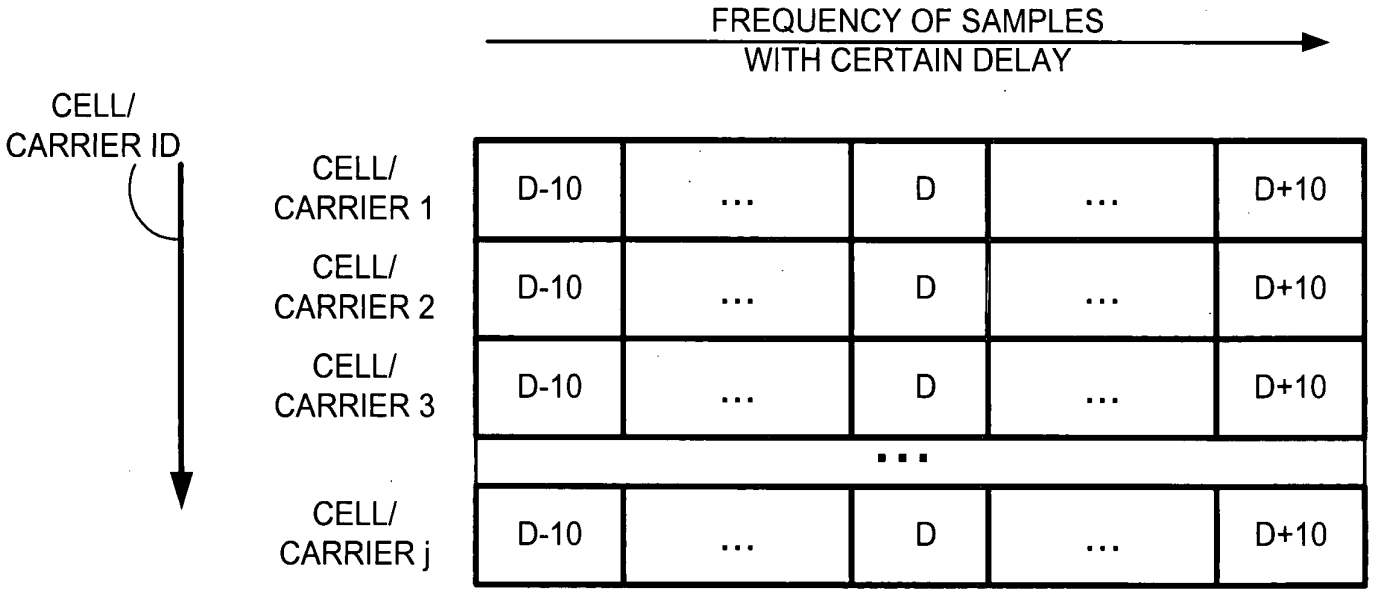


Fig. 14

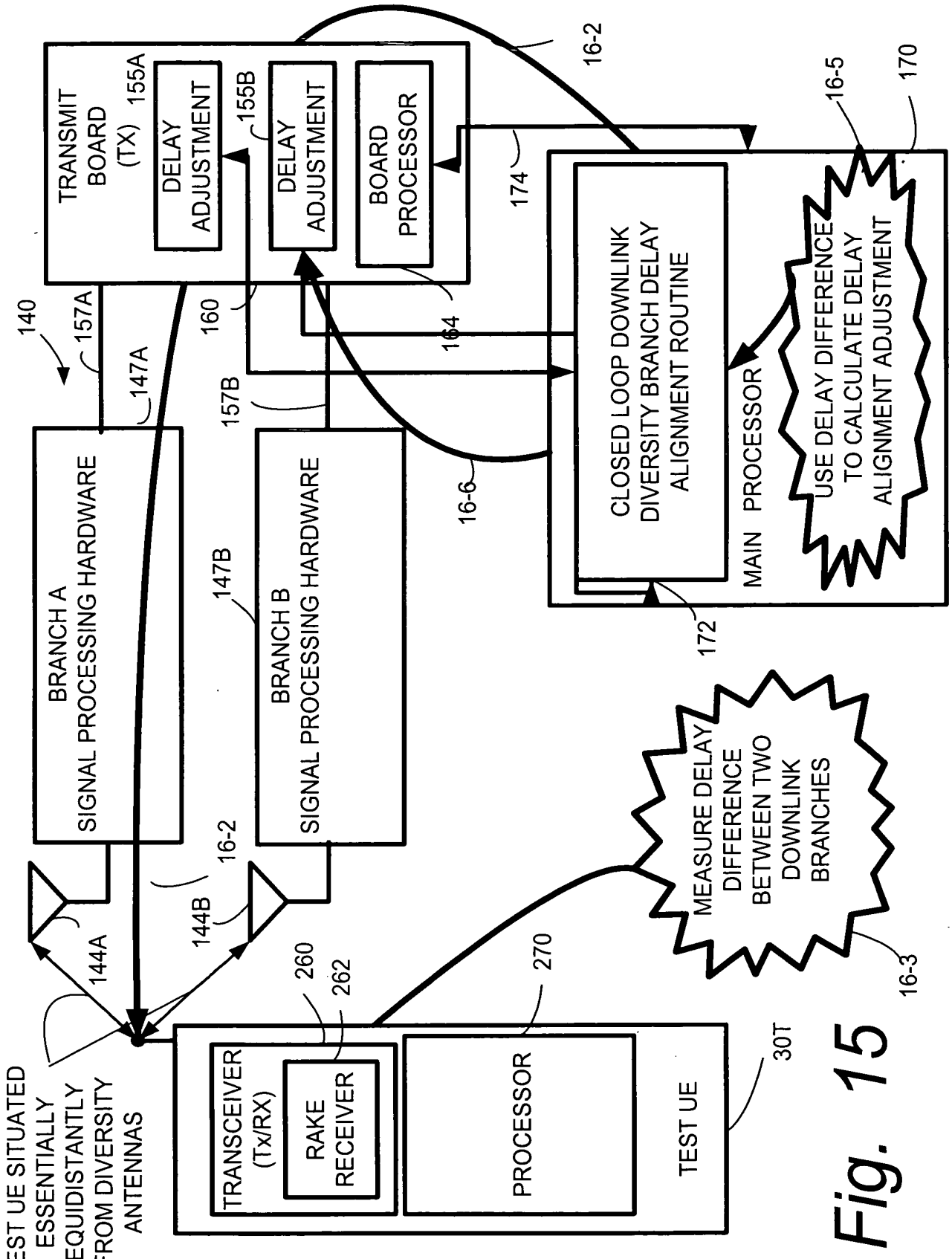

TRANSMIT BOARD (TX)
155A
DELAY ADJUSTMENT
155B
DELAY ADJUSTMENT
BOARD PROCESSOR
16-2
174
16-5
170
140
157A
147A
160
164
157B
CLOSED LOOP DOWNLINK DIVERSITY BRANCH DELAY ALIGNMENT ROUTINE
MAIN PROCESSOR
USE DELAY DIFFERENCE TO CALCULATE DELAY ALIGNMENT ADJUSTMENT
16-6
BRANCH A SIGNAL PROCESSING HARDWARE
147B
BRANCH B SIGNAL PROCESSING HARDWARE
172
MEASURE DELAY DIFFERENCE BETWEEN TWO DOWNLINK BRANCHES
16-2
144B
144A
260
262
270
16-3
TRANSCEIVER (Tx/RX)
RAKE RECEIVER
PROCESSOR
TEST UE
30T
TEST UE SITUATED ESSENTIALLY EQUIDISTANTLY FROM DIVERSITY ANTENNAS

Fig. 15

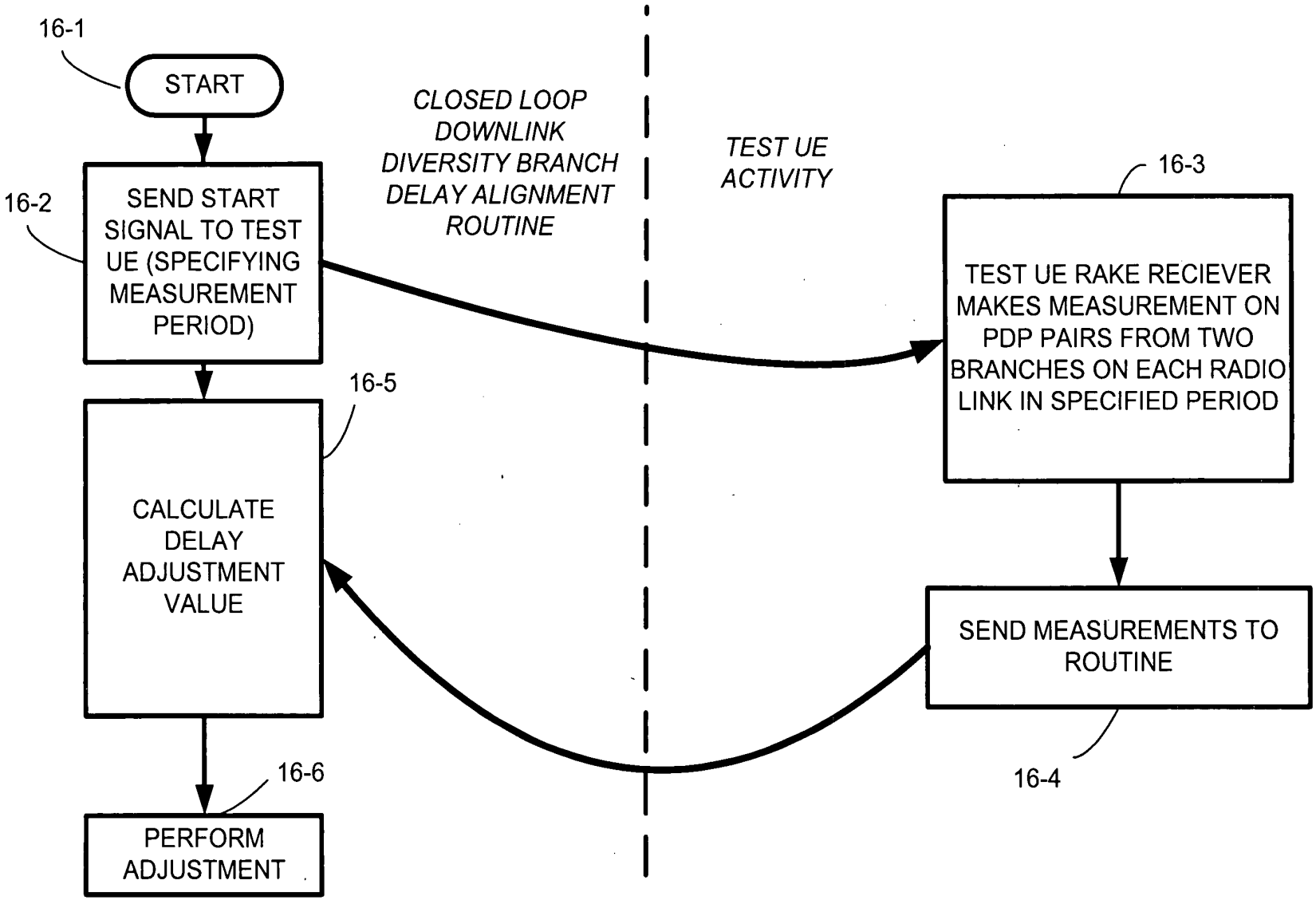


Fig. 16